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DERWENT-WEEK: 200172
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TITLE: Device of realizing cmos domino logic for improving
signal transmission
speed

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PATENT-FAMILY:

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APPLICATION-DATA:

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ABSTRACTED-PUB-NO: KR2001047544A

BASIC-ABSTRACT: NOVELTY - A device of realizing CMOS domino
logic for improving
signal transmission speed is provided to reduce the size of
the chip by
eliminating the inverter of each level and to speeding up the
signal
processing.

DETAILED DESCRIPTION - The circuit of realizing multiple
output domino
logic(400) includes a pair of multiple output domino logic
blocks(410,420). In
the front-end multiple output domino logic block(410), PMOS
devices for
discharging(411-1,411-2) and NMOS function
blocks(412-1,412-2) are connected to

be one-to-one.   When the clock signal(CK) is Low, the source voltage(Vdd) is
given to each NMOS function block(412-1,412-2).   The sources of the PMOS
devices(411-1,411-2) become the outputs of the front-end multiple output domino
logic block(410) without any inverter.   Here, when the clock signal(CK) is
High, the NMOS device(413) for discharging turns ON and discharges the NMOS
logic blocks(421-1,421-2).   In the back-end multiple output domino logic
block(420), when the inverted clock signal(CK') is High, the PMOS logic
blocks(422-1,422-2) are discharged.   The drains of the NMOS devices for
discharging(423-1,423-2) become the outputs of the back-end multiple output
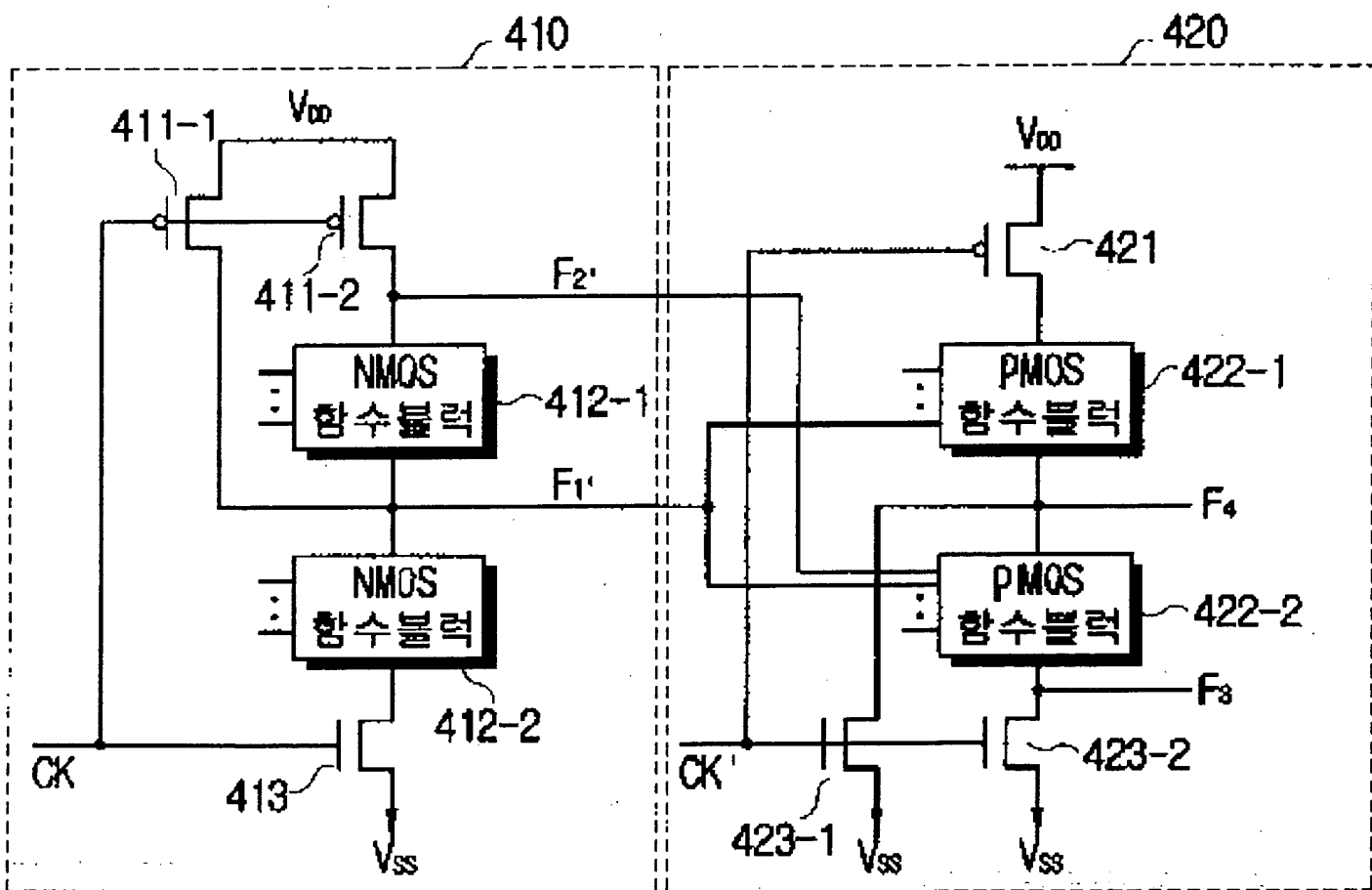domino logic block(420).

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS:
DEVICE CMOS DOMINO LOGIC IMPROVE SIGNAL TRANSMISSION SPEED

DERWENT-CLASS:   U21

EPI-CODES: U21-C;

400

410
411-1
$V_{DD}$
411-2
NMOS 함수블럭 412-1
$F_2'$
NMOS 함수블럭 412-2
$F_1'$
CK
413
$V_{SS}$

420
$V_{DD}$
421
PMOS 함수블럭 422-1
PMOS 함수블럭 422-2
$F_4$
$F_3$
423-2
CK
423-1 $V_{SS}$
$V_{SS}$

Han et al.